A Novel Dynamic Voltage Restorer based on Matrix Converters

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Abstract—**In this paper a Dynamic Voltage Restorer (DVR) based on a matrix converter without energy storage devices is proposed to cope with voltage fluctuations. The ac/ac power converter takes energy from the grid during voltage sag/swell. By connecting the matrix converter's input terminals on the load-side and injecting the compensation voltages on the supply-side, it is possible to hold a constant input voltage, resulting in an efficient solution for compensating deep voltage sags and swells. Thus, the proposed topology has the ability to compensate balanced and unbalanced voltage fluctuations and to eliminate the energy storage elements. The space-vector modulation (SVM) technique is utilized to fulfill the input and output requirements. Numerical simulation results are presented to validate the approach.**

Index Terms— Voltage Restorer (DVR), matrix converter (MC), voltage control.

I. INTRODUCTION

VOLTAGES in power distribution systems are commonly affected by disturbances. According to the Canadian Electric Associate (CEA) and the Electric Power Research Institute (EPRI), among various power quality problems the majority of events are associated with either a voltage sag or a voltage swell [1-2]. Such events are a common reason for failures in production plants, sensitive loads malfunctions, and economic losses [3]. Many solutions to these problems have been published in recent years. The existing methods include tap changers, FACTS devices such as the distribution STATCOM (D-STATCOM), the Unified Power Quality Controller (UPQC), and the Dynamic Voltage Restorer (DVR) [4-7]. The series compensation device DVR was introduced for voltage sag mitigation and has been adopted as a common solution to the problem. The DVR's operating principle is to inject the "missing" voltage in series with the supply in order to maintain an undisturbed load voltage, Fig. 1. Since the first DVR introduced in 1994, several topologies have been developed, along with different control methods and with harmonic compensation purposes [8-9]. Most of the DVR topologies presented in the literature [10] can be classified within two categories: (*i*) using stored energy (batteries, capacitors, flywheel, etc.) to supply the delivered power and, (*ii*) having no significant internal energy storage. In the latter case, the energy is taken from the faulted grid supply. These topologies share one same specific characteristic: the dc-link.

In order to eliminate the drawbacks imposed by the use of dc-link passive elements some researchers have focused their efforts to the topologies based on ac/ac power converters, which results in reduced maintenance requirements and improved power density [11-13]. DVR topologies with energy storage are highly favored to compensate deep level voltage sags in sensitive loads within a wide power factor range. However, this type of systems has significant drawbacks regarding complexity and overall cost (energy storage and power converter).

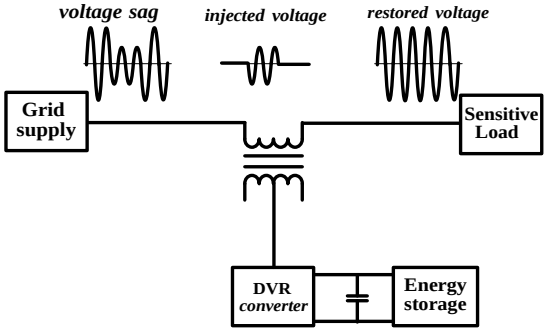

Figure 1. Principle of operation of the dynamic Voltage Restorer

Among the existing DVR topologies with energy storage in ac form, various different types of switching power converters have been employed, being the matrix converter an attractive solution due to its operative advantages. This paper proposes a novel DVR topology that takes advantage of the matrix converter operating characteristics, being able to compensate balanced and unbalanced voltage fluctuations as well as deep-level voltage sags. One of the advantages of the proposed system is the dc-link passive components, and ac energy storage devices elimination. The paper is organized as follows: the DRV topology is proposed in Section II; the matrix converter modulation strategy is covered in Section III; the DVR's operation controller and compensation strategy is described in Section IV; numerical simulations via detailed computer model and conclusions are presented in Section V and Section VI, respectively.

II. SYSTEM ARCHITECTURE

A. The ac/ac-based DVR

Conceptually, the DVR operates to maintain the load supply voltage at rated value. When the DVR injects a voltage, it exchanges active and reactive power with the electric system. To supply active power, the DVR requires a source. In the case of DVRs with ac/ac converters, there are two types of system to be considered. The first one, Fig. 2, has not significant energy storage.

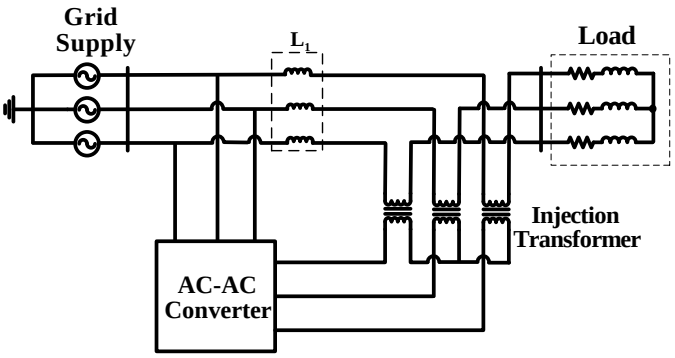

Figure 2. AC/AC DVR without energy storage devices

DVR topologies without external energy storage devices assume that a part of the supply voltage remains during the sag, and this residual supply can be used to generate the energy required to maintain full load power at rated voltage. Hence, the ability to compensate deep voltage sags will be limited by the input voltage. For instance, in [14] a VeSC-based DVR with this topology is proposed to mitigate symmetric voltage sags.

The second type of configuration, Fig. 3, uses stored energy to feed the required power. Topologies that store energy have an improved performance compared with the no-energy storage solution but the cost is higher. In [12] a matrix converter-based DVR using flywheel energy storage, is proposed for deep-level symmetric sags

B. DVR'S matrix converter-basedwith no-ebergy storage

The proposed topology is developed in order to fulfill the next requirements:

1) The converter must have the ability to compensate balanced and unbalanced deep-level voltage variations.
2) Minimization of cost and operational complexity without energy storage devices.

Based on these two requirements, the topology in Fig. 4 has been developed. In this configuration, the energy is taken from the incoming supply and the matrix converter input terminals are connected in the load-side. In this way, the controller's input voltage can be held almost constant by injecting sufficient voltage ($\underline{V}_i$). If the DVR is connected to a robust grid, the power to the load can be ensured by increasing the supplied current, injecting the missing voltage.

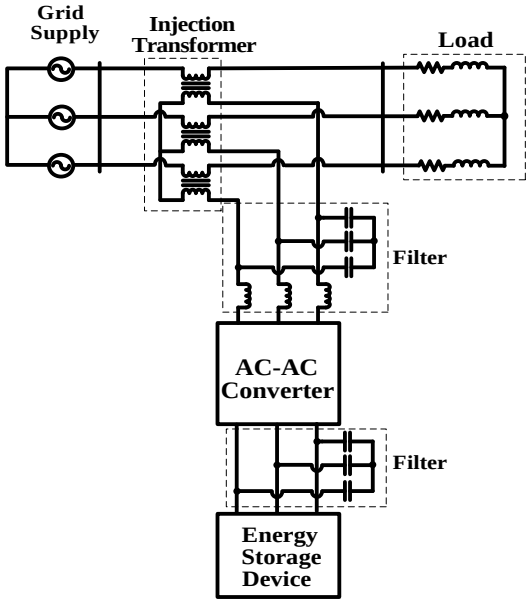

Figure 3. AC/AC DVR without energy storage devices

Hence,

$$\underline{V}_{im} \approx \left|\underline{V}_l\right| \approx \left|\underline{V}_s + \underline{V}_i\right| \quad (1)$$

where:

$\underline{V}_{im}$ = Matrix converter input voltages

$\underline{V}_l$ = Load voltages

$\underline{V}_s$ = System voltages

$\underline{V}_i$ = Injected voltages

The current rating increases because it supplies current into the matrix converter as well as into the load. This topology has the disadvantage of larger currents in the supply system and the negative grid effects caused by the harmonic distorted currents drawn by the converter. However, with the appropriate modulation scheme, the matrix converter can be an efficient solution in terms of voltage compensation

III. MATRIX CONVERTER MODULATION

Although matrix converter was initially introduced as an AC Driver, due to its advantages may be used in voltage compensation applications. The main matrix converter disadvantages are the limited voltage transfer ratio and the converter's sensitivity to disturbances in the input voltages. In [15], it has been demonstrated that through the instantaneous value measurement of two line-to-line input voltages, it is possible to produce balanced and sinusoidal output voltages, even under unbalanced input voltages. Nevertheless, taking into account the input/output power balance equation, it is possible to determine that non-sinusoidal input currents will appear.

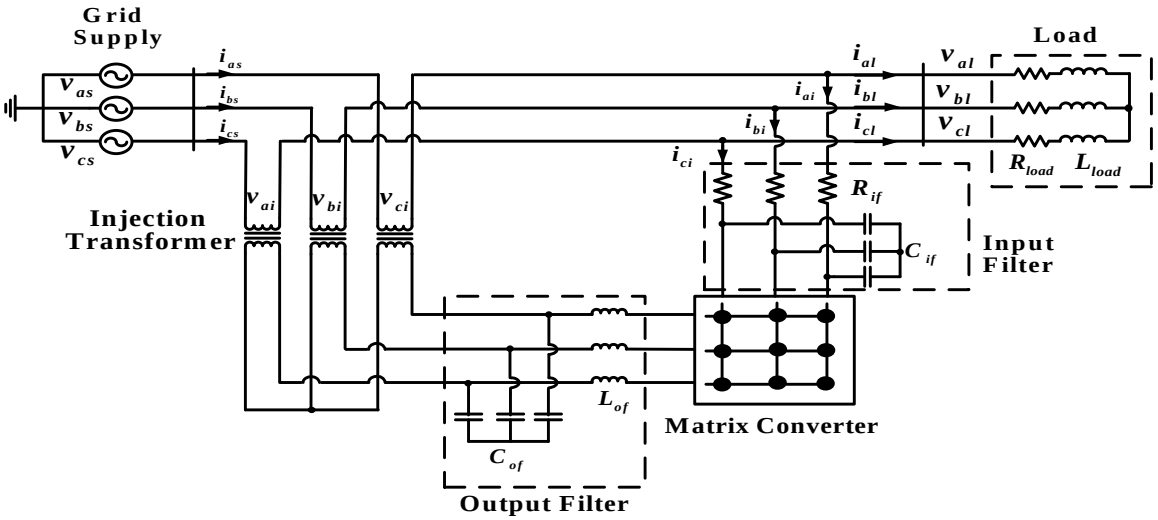

Figure 4. Proposed DVR system architecture

The matrix converter in Fig. 5 consists of nine bi-directional switches arranged in three groups, each being associated with an output line. This bi-directional switches arrangement connects any of the input lines to any of the output lines. A matrix with elements S*ij*, representing the state of each bi-directional switch (*on=1, off=0*), can be used to represent the matrix output voltages (v_u, v_v, v_w) as functions of the input voltages (v_a, v_b, v_c) as follows,

$$\begin{bmatrix} v_u \\ v_v \\ v_w \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{2}$$

The input phase currents (i_a, i_b, i_c) can be related to the output phase currents (i_u, i_v, i_w) by,

$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} S_{11} & S_{21} & S_{31} \\ S_{12} & S_{22} & S_{32} \\ S_{31} & S_{23} & S_{33} \end{bmatrix} \begin{bmatrix} i_u \\ i_v \\ i_w \end{bmatrix} \tag{3}$$

As can be seen in (2)-(3), the matrix output voltages-matrix input currents control is not independent.

A. Direct Space Vector Pulse Width Modulation (DSVPWM) for unbalanced and distorted voltage supply

In the control vector algorithms reported in [16-18], the three-phase framework is mapped into a complex vector in terms of the αβ coordinates. The control strategy implies the modification of the amplitude and phase of the reference vector, from which the switches' triggering pulses are determined. The modulation technique used in this paper is the one presented in [15], which performs the power conversion directly from *ac* to *ac* and is capable to cope with distorted input voltages. It is known that in matrix converters there are 21 switching configurations that can be utilized in DSVPWM. Among these, 18 are active switching configurations, which determine output voltage vectors having fixed direction. These are represented in Figs. 7-8 by the space vectors *E2, E3, E4, E5, E7, E9, E10, E11, E13, E15, E17, E18, E19, E21, E23, E24, E25*, and *E26*.

The four basic equations that satisfy, at the same time, the requirements of the line-to-line voltage vector $\overline{U}_{out(ref)}$ and input current vector $\overline{I}_{in(ref)}$, can be expressed as follows:

$$\overline{U}'_{out(ref)} = \left(\overline{U}^{I}_{out} m_I\right) + \left(\overline{U}^{II}_{out} m_{II}\right) \tag{4}$$

$$\overline{U}''_{out(ref)} = \left(\overline{U}^{III}_{out} m_{III}\right) + \left(\overline{U}^{IV}_{out} m_{IV}\right) \tag{5}$$

$$\overline{I}'_{in(ref)} = \left(\overline{I}^{II}_{in} m_{II}\right) + \left(\overline{I}^{IV}_{in} m_{IV}\right) \tag{6}$$

$$\overline{I}''_{in(ref)} = \left(\overline{I}^{I}_{in} m_I\right) + \left(\overline{I}^{III}_{in} m_{III}\right) \tag{7}$$

$\overline{U}'_{out(ref)}$, $\overline{U}''_{out(ref)}$ are the voltage vector components of the reference vector $\overline{U}_{out(ref)}$, Fig.7. $m_j, \overline{U}^{j}_{out}, \overline{I}^{j}_{in}$ are the duty cycle, the output voltage vector, and the input current vector, respectively, related to the four switching configurations for each switching period (j = *I, II, III, IV*).

With reference to the case shown in Figs. 6-7, solving (4)-(7), the corresponding duty cycles become,

$$m_I = \frac{2}{\sqrt{3}} \frac{\left|\overline{U}_{out(ref)}\right|}{\left|\overline{U}_{in}\right|} \frac{\cos\left(\angle\overline{U}_{out(ref)} - \frac{\pi}{3}\right)\cos\left(\frac{\pi}{3} + \angle\overline{I}_{in(ref)}\right)}{\cos\theta_{in}} \tag{8}$$

$$m_{II} = \frac{2}{\sqrt{3}} \frac{\left|\overline{U}_{out(ref)}\right|}{\left|\overline{U}_{in}\right|} \frac{\cos\left(\angle\overline{U}_{out(ref)} - \frac{\pi}{3}\right)\cos\left(\frac{\pi}{3} - \angle\overline{I}_{in(ref)}\right)}{\cos\theta_{in}} \tag{9}$$

$$m_{III} = \frac{2}{\sqrt{3}} \frac{\left|\overline{U}_{out(ref)}\right|}{\left|\overline{U}_{in}\right|} \frac{\cos\left(\angle\overline{U}_{out(ref)} + \frac{\pi}{3}\right)\cos\left(\frac{\pi}{3} + \angle\overline{I}_{in(ref)}\right)}{\cos\theta_{in}} \tag{10}$$

$$m_{IV} = \frac{2}{\sqrt{3}} \frac{|\overline{U}_{out(ref)}|}{|\overline{U}_{in}|} \frac{\cos\left(\angle\overline{U}_{out(ref)} + \frac{\pi}{3}\right)\cos\left(\frac{\pi}{3} - \angle\overline{I}_{in(ref)}\right)}{\cos\theta_{in}} \quad (11)$$

The last expressions are valid within the intervals:

$$-\frac{\pi}{6} < \angle\overline{U}_{out(ref)} < \frac{\pi}{6}\,,\; -\frac{\pi}{6} < \angle\overline{I}_{in(ref)} < \frac{\pi}{6} \quad (12)$$

It is necessary to verify,

$$m_I + m_{II} + m_{III} + m_{IV} \le 1 \quad (13)$$

The zero vectors are applied to complete the cycle switching period.

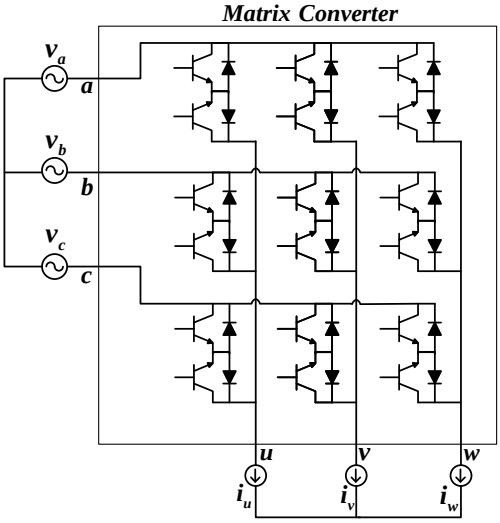

Figure 5. Direct Matrix Converter Topology

The scheme described by (8)-(11) is based on the assumption that the supply voltages are balanced without harmonics. It is known that when the supply voltage is unbalanced and/or distorted, the matrix operation converter can be affected by the generation of output voltages and currents which are also unbalanced and distorted. To overcome such a shortcoming, is necessary to modify the duty cycles relations, by incorporating the characteristics of the supply voltages into the computation and adjusting the calculated duty ratios accordingly [15]. Considering a unity power factor at the converter input terminals, the compensated duty cycles for each of the six sectors, are summarized in Tables 1-3, where K_i (i = I, II, III, IV, V, VI) is the sector in which the input current vector is located. This compensation method is simple to implement and has a fast dynamic response.

IV. CONTROLLER DESIGN

Output voltages v_u, v_v and v_w depend on the value of input voltages v_a, v_b and v_c, as was stated in (2). In the matrix converter, the voltage transfer ratio is given by [18],

$$\left|\overline{U}_{out}\right|_{MAX} \le \sqrt{3}/2 \left|\overline{U}_{in}\right|_{MIN} \quad (26)$$

Fig. 8 depicts this limitation for balanced and unbalanced input voltages. Thus, it is necessary to have the bigger region of available voltage, (Fig. 8 top), for properly operation under such conditions.

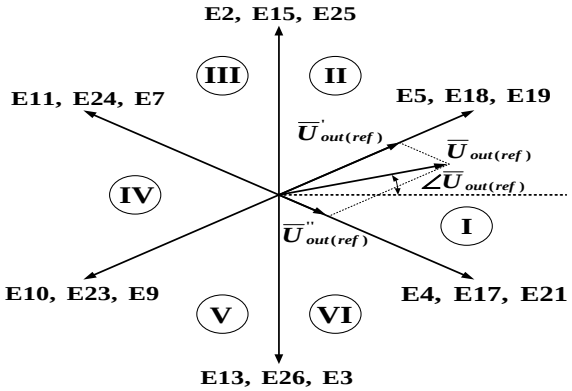

Figure 6. Fix vectors of the output-voltage

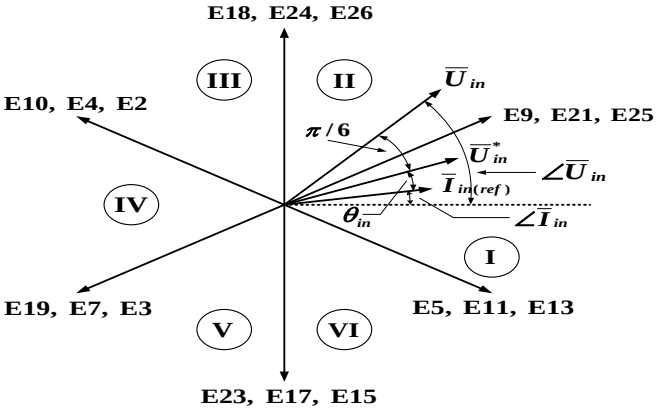

Figure 7. Fix vectors of the input-current

According to the proposed topology (Fig. 4), even with a severe sag condition in the supply voltage, the converter theoretically can inject as much as 80% of nominal voltage, by the proper control structure. Two control methods may generally be used for DVRs, being either open-loop control, or closed-loop control. Closed loop control was used for this testing system incorporating a rotating *dq* reference frame with feed-forward compensation. Fig. 9 displays the control loop structure. For example, consider a symmetric sag condition in the supply voltage, Fig. 4. The voltage sag factor n is defined as $n = v_{msag} / v_{ml}$, where v_{msag} is the magnitude of the supply voltage during the sag and v_{ml} is the magnitude of the rated load voltage.

Voltages are defined as,

$$\underline{V}_s = [v_{as}, v_{bs}, v_{cs}]^T \quad (27a)$$
$$\underline{V}_{ls} = [v_{abs}, v_{bcs}, v_{cs}]^T \quad (27b)$$
$$\underline{V}_r = [v_{abr}, v_{bcr}, v_{car}]^T \quad (27c)$$
$$\underline{V}_{load} = [v_{abl}, v_{bcl}, v_{cal}]^T \quad (27d)$$

where $\underline{V}_s$ = phase system voltages, $\underline{V}_{ls}$ = line-to-line system voltages, $\underline{V}_r$ = line-to-line reference voltages, $\underline{V}_{load}$ = line-to-line load voltages.

TABLE I. DUTY CYCLES WHEN K_I = I AND IV

K_I = I and IV	
$m_I = (-1)^{K_I} \frac{\lvert\overline{U}_{out(ref)}\rvert}{\lvert\overline{U}_{in}\rvert^2} \sin\left(\frac{\pi}{3} - \alpha_{out}\right)\left(v_{bc}(t) - v_{ab}(t)\right)$	(14)
$m_{II} = (-1)^{K_I} \frac{\lvert\overline{U}_{out(ref)}\rvert}{\lvert\overline{U}_{in}\rvert^2} \sin\left(\alpha_{out}\right)\left(v_{bc}(t) - v_{ab}(t)\right)$	(15)
$m_{III} = (-1)^{K_I} \frac{\lvert\overline{U}_{out(ref)}\rvert}{\lvert\overline{U}_{in}\rvert^2} \sin\left(\alpha_{out}\right)\left(v_{ca}(t) - v_{bc}(t)\right)$	(16)
$m_{IV} = (-1)^{K_I} \frac{\lvert\overline{U}_{out(ref)}\rvert}{\lvert\overline{U}_{in}\rvert^2} \sin\left(\frac{\pi}{3} - \alpha_{out}\right)\left(v_{ca}(t) - v_{bc}(t)\right)$	(17)

TABLE II. DUTY CYCLES WHEN K_I = II AND V

K_I = II and V	
$m_I = (-1)^{K_I} \frac{\lvert\overline{U}_{out(ref)}\rvert}{\lvert\overline{U}_{in}\rvert^2} \sin\left(\frac{\pi}{3} - \alpha_{out}\right)\left(v_{ab}(t) - v_{ca}(t)\right)$	(18)
$m_{II} = (-1)^{K_I} \frac{\lvert\overline{U}_{out(ref)}\rvert}{\lvert\overline{U}_{in}\rvert^2} \sin\left(\alpha_{out}\right)\left(v_{ab}(t) - v_{ca}(t)\right)$	(19)
$m_{III} = (-1)^{K_I} \frac{\lvert\overline{U}_{out(ref)}\rvert}{\lvert\overline{U}_{in}\rvert^2} \sin\left(\alpha_{out}\right)\left(v_{bc}(t) - v_{ab}(t)\right)$	(20)
$m_{IV} = (-1)^{K_I} \frac{\lvert\overline{U}_{out(ref)}\rvert}{\lvert\overline{U}_{in}\rvert^2} \sin\left(\frac{\pi}{3} - \alpha_{out}\right)\left(v_{bc}(t) - v_{ab}(t)\right)$	(21)

TABLE III. DUTY CYCLES WHEN K_I = III AND VI

K_I = III and VI	
$m_I = (-1)^{K_I} \frac{\lvert\overline{U}_{out(ref)}\rvert}{\lvert\overline{U}_{in}\rvert^2} \sin\left(\frac{\pi}{3} - \alpha_{out}\right)\left(v_{ca}(t) - v_{ab}(t)\right)$	(22)
$m_{II} = (-1)^{K_I} \frac{\lvert\overline{U}_{out(ref)}\rvert}{\lvert\overline{U}_{in}\rvert^2} \sin\left(\alpha_{out}\right)\left(v_{ca}(t) - v_{ab}(t)\right)$	(23)
$m_{III} = (-1)^{K_I} \frac{\lvert\overline{U}_{out(ref)}\rvert}{\lvert\overline{U}_{in}\rvert^2} \sin\left(\alpha_{out}\right)\left(v_{ab}(t) - v_{ca}(t)\right)$	(24)
$m_{IV} = (-1)^{K_I} \frac{\lvert\overline{U}_{out(ref)}\rvert}{\lvert\overline{U}_{in}\rvert^2} \sin\left(\frac{\pi}{3} - \alpha_{out}\right)\left(v_{ab}(t) - v_{ca}(t)\right)$	(25)

For the DSVPWM implementation is necessary to transform input and output voltages into αβ coordinates. So that, the input, load, and reference voltages can be represented by,

$$\underline{V}_{ls\alpha\beta} = \left[T_{\alpha\beta}\right]\left[\underline{V}_{ls}\right] \tag{28a}$$

$$\underline{V}_{load\alpha\beta} = \left[T_{\alpha\beta}\right]\left[\underline{V}_{load}\right] \tag{28b}$$

$$\underline{V}_{r\alpha\beta} = \left[T_{\alpha\beta}\right]\left[\underline{V}_{r}\right] \tag{28c}$$

where,

$$T_{\alpha\beta} = \begin{bmatrix} -1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & \sqrt{3}/2 \end{bmatrix} \tag{29}$$

The injected voltage generated by the matrix converter depends on the duty cycles value. Then, the main control variables are $\lvert\overline{U}_{out(ref)}\rvert$ and $\lvert\overline{U}_{in}\rvert$ from (14)-(25), corresponding to the injection voltage required and voltage at the input terminals of the converter magnitudes, respectively.

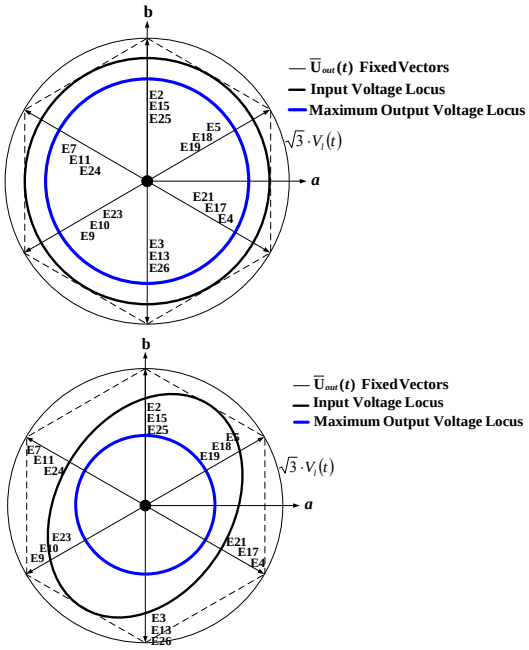

Figure 8. Top: Voltage vectors for balanced input voltage condition. Bottom: Voltage vectors for unbalanced conditions (sag of 50% on phase b)

The DVR is synchronized to the grid supply through a phase-locked loop (PLL). A relatively slow PLL is used to limit the influence of harmonics and nonsymmetrical input voltages. Taking the phase angle estimated by the PLL, the voltages are transformed into the d-q coordinates. At the instant that supply voltage goes down, the feed forward control generates one error signal as follows:

$$\underline{e}_1 = \left[\underline{V}_{rdq}\right] - \left[\underline{V}_{sdq}\right] \tag{30}$$

The feed-back loop generates the PI controller's input,

$$\underline{e}_2 = \left[\underline{V}_{rdq}\right] - \left[\underline{V}_{loaddq}\right] \tag{31}$$

To generate the duty cycles for compensation, an inverse transformation has to be performed in order to compute the error signals, $\underline{e}_1$ and $\underline{e}_2$, in terms of αβ coordinates. Then, the injection voltage needs to be,

$$\left|\overline{U}_{out(ref)}\right| = \left|e_{1\alpha\beta}\right| + K_p\left|e_{2\alpha\beta}\right| + K_i\int\left|e_{2\alpha\beta}\right| \quad (32)$$

verifying that $\left|\overline{U}_{out(ref)}\right| \le \sqrt{3}/2\left|\overline{U}_{in}\right|$.

Using the proposed method, the injection voltage waveforms reduce the harmonic components.

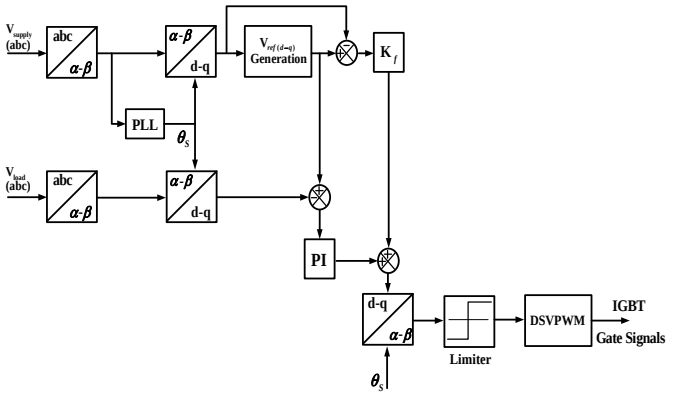

Figure 9. Scheme of the output voltage control based on the PI controller

V. SIMULATION

The time-domain performance of the whole DVR system is verified by detailed numerical simulation using PSCAD software. The system key parameters are given in Table 4. The matrix converter-based DVR is utilized for voltage sag and swell compensation. Two different tests have been carried out. In test 1, mitigation of balanced sag is evaluated. In test 2 the performance of DVR is confirmed for unbalanced voltage sag.

For the case of balanced sag, a 40% three-phase voltage sag in the supply voltage is simulated, lasting for 0.08s. Voltage and current waveforms during the voltage sag period are plotted in the *abc* reference frame, Figs. 10-11. It can be observed that the DVR is able to maintain the voltage load almost undisturbed during the sag period, by injecting the appropriate compensation. The harmonic content of the injected voltage in Fig. 10 is due to the current flowing into the converter which leads a distorted generated voltage. The fast response of the control is illustrated through the load current plot in which the signals do not show any disturbance. The currents flowing from the supply into the matrix converter increase during the sag, but both currents shows not considerable harmonic distortion as expected.

TABLE IV. LIST OF PARAMETERS

Parameter	Value
C_{if}: Input Filter Capacitor	50 μF
R_{if}: Input Filter Resistance	1 Ω
C_{of}: Output Filter Capacitor	6 μF
L_{of}: Output Filter Inductor	1.2 mH
L_{load}: Load Inductor	33.6 mH
R_{load}	20 Ω

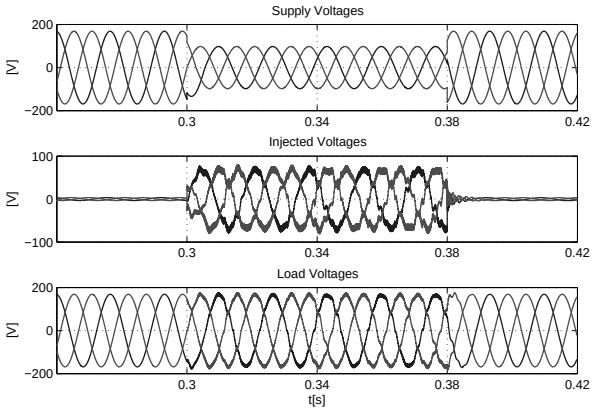

Figure 10. DVR response for balanced voltage sag compensation: Supply voltages, Injected voltages, and Load voltages.

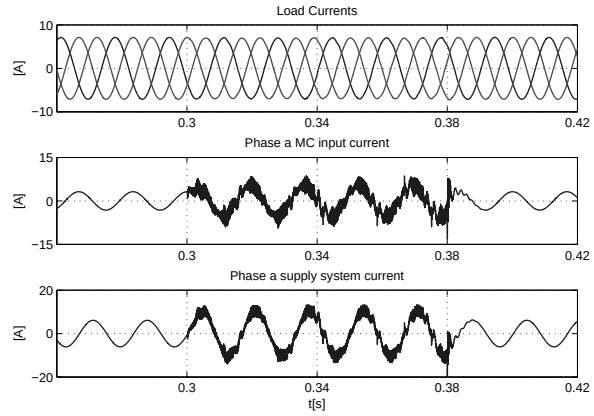

Figure 11. DVR response for balanced voltage sag compensation: Load currents, Phase *a* matrix converter input current, Phase *a* supply system current.

In the second test, the DVR performance is investigated under an unbalanced voltage variation. For this test, voltage sags of 20% and 40% in phase *b* and phase *c*, respectively, are considered. Furthermore, a 17% voltage swell is applied on phase *a*. The DVR response for unbalanced test is illustrated in Figs. 12-13. The matrix converter generates the needed voltage components to compensate the load voltages. The load voltage is in this case fully maintained, which demonstrate the effectiveness of this proposition. The supplied system currents show a higher harmonic content compared with the previous study case because of the low order harmonics generated in the drawn currents by the matrix converter. However this condition does not affects the overall performance.

VI. CONCLUSIONS

This paper has presented a novel DVR system topology employing a matrix converter without energy storage. In this topology, the matrix converter input terminals are connected on the load-side, characteristic that makes it able to generate the voltages for unbalanced and deep voltage sags compensation. The overall system encompassing the voltage injection controller and the plant have been simulated via detailed PSCAD model. In spite of negative grid effects caused by non linear currents drawn by the matrix converter,

the time domain waveforms demonstrate the acceptable dynamic response in voltage compensation applications. The system proposed has been evaluated as a good option because of its acceptable performance, relative low cost and complexity.

The next step in this research is to support the present theoretical analysis by experimental results.

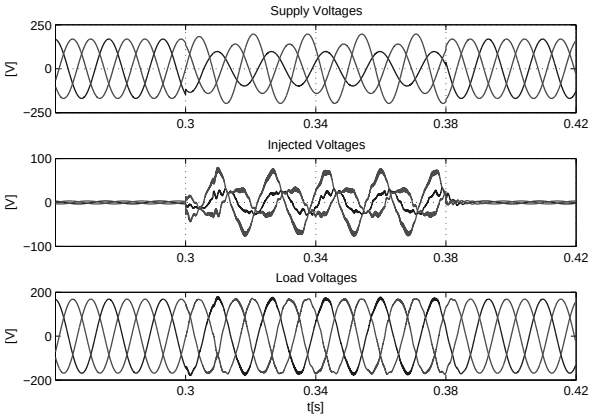

Figure 12. DVR response under unbalanced voltage variation: Supply voltages, Injected voltages, and Load voltages.

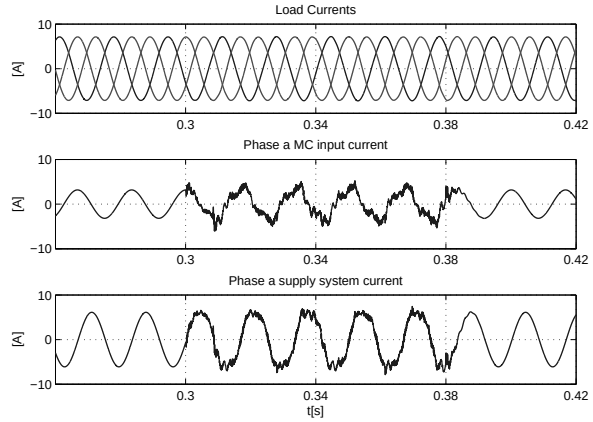

Figure 13. DVR response under unbalanced voltage variation: Load currents, Phase *a* matrix converter input current, Phase *a* supply system current.

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