Partial Discharge Detection System for Counting PD Signals In High Voltage Underground Cable by using FPGA Technology

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Abstract— Currently, FPGA (Field Programmable Gate Array) technology is being widely used for signal processing and control owing to its fast digital processing capability. We have recently developed successfully a high-speed data acquisition system that combines a commercial FPGA board (ML405) with the high speed ADC in ADC 083000RB that has 8 bit pairs LVDS in resolution, sampling rate of 3 GS/s and bandwidth of 3 GHz for counting very high speed transient signals. The programming is in VHDL. This system enables direct measurement and counting of transient signals at 1-10 ns pulse width at a sampling frequency 3 GHz. The partial discharge (PD) signals in this work are simulated by using Pico Pulse generator. All the counting is performed in the FPGA without the use of oscilloscope. The count rates are displayed in the LCD monitor of the FPGA hence rendering it to be highly mobile.

Keywords- *Partial Discharge Detection, Magnitude Field, FPGA Technology, Peak Detector, Real Time Processing, Underground Cable, Portable Detector, VHDL Programming, ADC 083000RB 3GSPS.*

1. INTRODUCTION

PD detection system is an automatic system that can detect and display PD signals from underground cable for easy readout. This system can work without an oscilloscope, computer or any other associated costly measuring equipment. The PD signal is detected by using magnetic probe sensor. This system can detect the PD signal in high voltage underground cable from above the ground without cutting off the flow of electricity to underground cables. Figure 1 shows block diagram connection of the ADC in ADC083000RB 3GS/s and LCD of the FPGA Board.

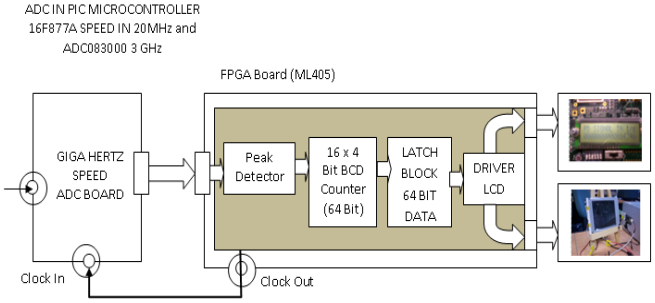

Figure 1 Block diagram connection of the ADC in microcontroller and LCD of the FPGA board

The PD detection circuit system is created by using and developed a high-speed data acquisition system that combines a commercial FPGA (ML405 board) XC4VFX20 Xilinx Virtex 4 with a fast ADC (ADC083000RB; 8 bit pairs LVDS; maximum sampling rate: 3 GS/s; bandwidth: 3 GHz).

The PD detection sensor is created by using magnetic probe. The magnetic probe is the sensor that detects the fast transient PD signal. The probe has 3D axis, in the x, y and z directions. The probe is designed to detect very fast transient signals. The probe is integrated to the PD detection circuit.[1] The circuit uses ADC to digitized the fast transient signal and FPGA to perform the counting. The PD detection circuit system consists of peak detector block, BCD counter 64 bit block, reset automatic block, 64 bit latch block, 16 character text display block, 16 counter display block, driver LCD 16x2 character module block and driver LCD graphic color TFT block.

2. CONSTRUCTION OF HIGH-SPEED DATA ACQUISITION SYSTEM

The high-speed data acquiring system is composed of an ADC board (ADC083000RB) and an FPGA board (ML405 board). The ADC stores real time data in the FPGA board for analyzing and counting the real time PD signal detected by the peak detector block and the 64 bit BCD counter block. Then the real time data is transmitted to the latch block in order for the data not to change until the data is updated each 1 second (Figure 1). The FPGA board stores result of counted PD signal data to LCD 16x2 character module in FPGA board and external LCD. Figure 2 shows the ML501 board installed in a box together with ADC083000 RB reference board.

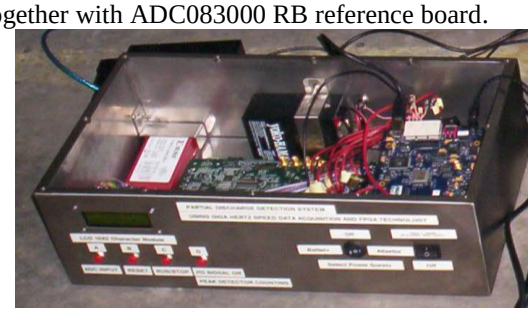

Figure 2 The connection of the Giga Hertz speed ADC board and FPGA ML405 board Xilinx Virtex 4

ADC083000RB

ADC083000RB is a reference/evaluation board equipped with an ADC083000RB 8-bit analog to digital converter ADC manufactured by National Semiconductors which can operate at speeds up to 3.4 GSPS. This evaluation board is used with National Semiconductors wave vision (version 4) software to analyze the data. Its features are as follows:

- Resolution: 8 bit pairs (totally 16 bits each port of 4 ports)
- Maximum sampling rate: 3GSPS
- Analog bandwidth: 3 GHz
- Data output: LVDS compatible

ML405

ML405 board is a commercial FPGA board manufactured by Xilinx and is equipped with a Virtex-4 Its features are as follows:

- RS232 serial connector to PC.
- DDR2-SDRAM.
- LVDS interface connector 16 bit differential I/O.
- LCD 16X2 Character Module in FPGA board
- 5 Push button connection with 5 led of push button.
- 4 led GPIO connection
- 32 FPGA pins I/O single ended connection for connection to external LCD 16x2 character module and 8 bit LVDS input real time data from ADC083000RB.

Figure 3 The connection of the FPGA ML405 board Xilinx Virtex 4 and PC are connected by JTAG USB II cables via adaptors for upload the VHDL

The ML405 and the PC are connected by JTAG USB II cables via adaptors for upload the VHDL, as shown in Figure 3.

3. DESIGN OF FPGA LOGIC

Figure 3 shows how to upload the VHDL program from PC using JTAG USB II cable to FPGA. Xilinx ISE 10.1 version, an integrated development tool, has been utilized for designing the FPGA logic. The program is synthesized using Xilinx Synthesize Technology (XST) before running and implementation in FPGA platform.[2]

LVDS Interface

Virtex4 has input-buffers and output-buffers which can handle single-end signal and differential signals. The ML405 board has 32 bit single end I/O interface and ML405 is equipped with 8 pairs connectors as the LVDS interface to ADC083000.

The ML405 board has an expansion header with 16 LVDS capable differential pairs, 14 spare I/Os shared with pushbutton switches and LEDs, power, JTAG chain expansion capability, and IIC bus expansion.

The ADC 083000RB has an expansion header to external equipment with 16 LVDS capable differential pairs, and has an internal port connection to PC by USB with 32 LVDS capable differential pairs. The ADC083000RB consisting of expansion header to external equipment with 16 LVDS capable differential pairs in left side of the ADC board, as shown in Figure 4.

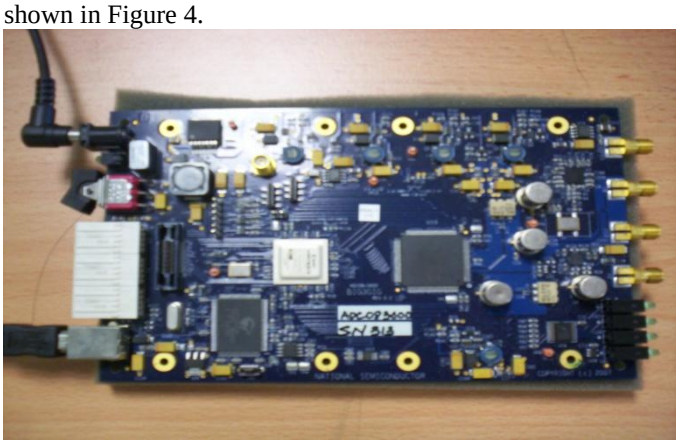

Figure 4 The expansion header to external equipment with 16 LVDS capable differential pairs in ADC083000RB

Data Acquisition and Real Time Data

A built-in peak detector block Virtex-4 has been used to accumulate the acquired data. The ADC and peak detector block is designed to receive 8 bits single-end real time data from ADC in ADC083000RB and then the peak of pulse signal is detected by the peak detector block in FPGA board by using XST (Xilinx Synthesize Technology) in ISE10.1 and Xilinx ISE Implement Design. At a sampling frequency of 3 GHz, the FPGA can accumulate pulse signal data with duration of 1 to 10 ns. The data accumulation peak detector is controlled by the threshold value in the VHDL programming.

Block Programming in FPGA Technology

1. The ADC and Peak Detector Block in Hardware of FPGA Board:

The function of this ADC and peak detector block is to receive very high speed data logic from ADC module after the data is converted from analogue pulse signal and then detect the amount of peak pulse signals in logic data when processed by the peak detector in FPGA board.

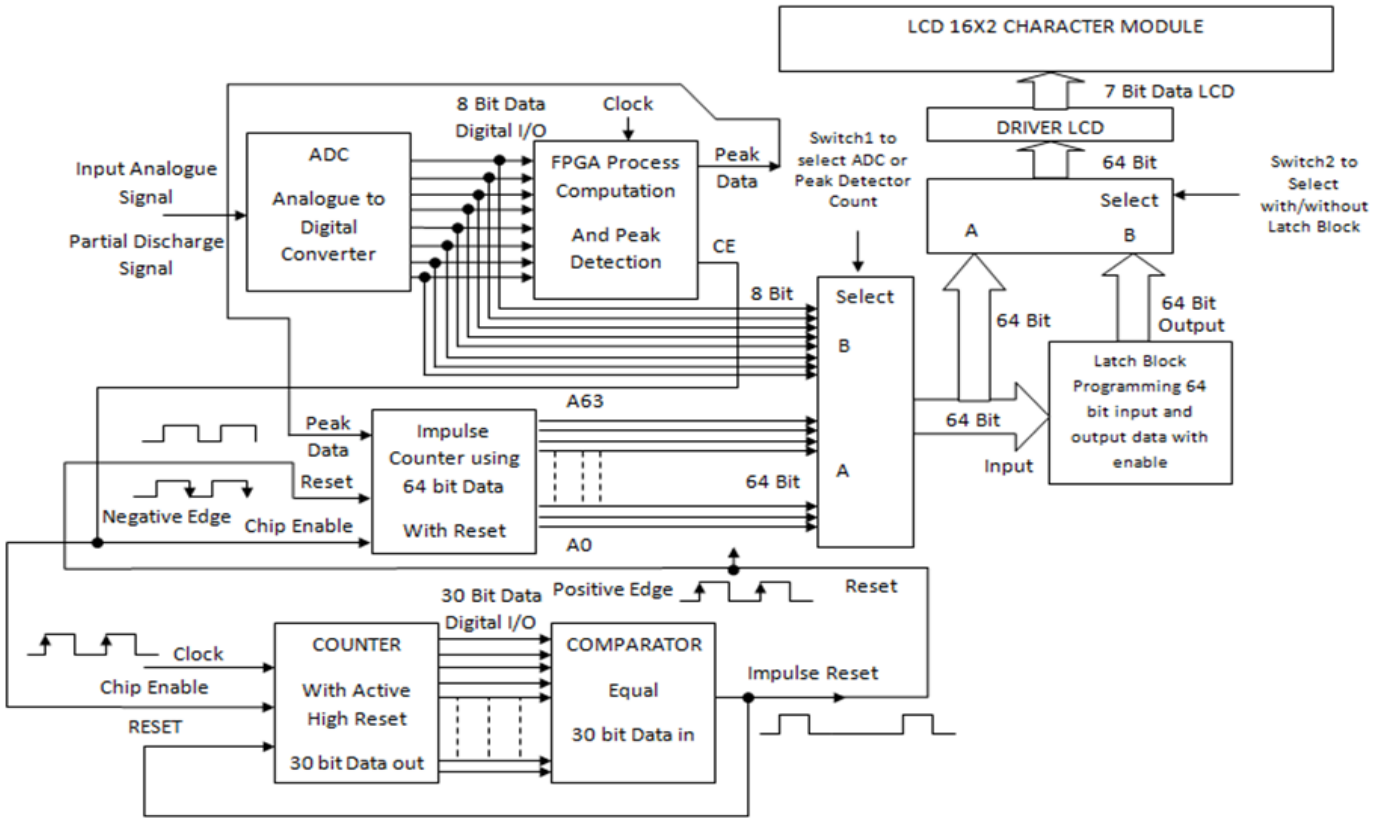

Figure 5 The Block Diagram Complete of PD Detection Circuit System in FPGA Board

Figure 5 shows the complete construction block diagram of the PD detection circuit system in FPGA logic. The peak detector in this system is using the threshold method. Figure 6 shows the simulated transient pulse and the threshold value set by the peak detector block. In this simulation the peak detector is designed to have a 196 decimal or 11000100 bin threshold voltage. Set at 196 is the best value of the lowest threshold value using ADC083000RB 3GHz. It means that if the input signal is more than 2.8 mV or 11000100 bin, the output of the peak detector is logic 1 in LVDS data and if input signal is less than 2.8 mV or 11000100 bin, the output peak detector is logic 0 or 0 V. The threshold value can be changed by changing the logic data of the threshold value in VHDL programming.

The input analogue data of ADC083000RB has maximum voltage 150 mV and minimum voltage -150mV.

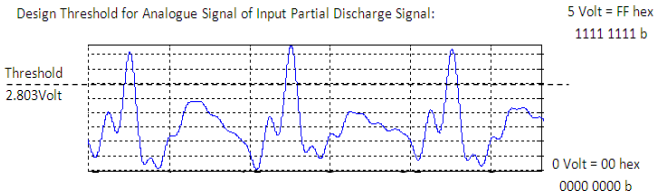

Figure 6 Design Threshold value in Peak detector Block

The real time PD signal is simulated by an impulse generator (PicoPulse). The source PD signal shows in figure 7.

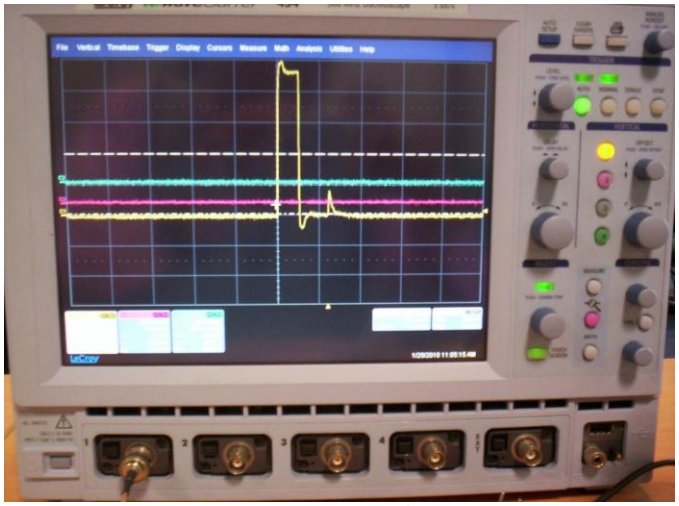

Figure 7 Partial Discharge (PD) signal from impulse generator

After finishing the processing of the peak detector, the output data in this block will be sent to BCD Counter with reset block.

2. The BCD Counter with reset block in hardware of FPGA board:

The purpose of the BCD Counter and reset block is for counting the amount of PD signals from the ADC signal and peak detection block in the FPGA and then perform the

computation of the real time data using 64 bit digital output data in VHDL Programming.

The BCD Counter will return back to 0 if the reset of counter is active. In this VHDL programming, the counter is designed using reset active high (type negative edge reset) for up counter in the FPGA board. It means there are 16 BCD counter used in the system to detect amount of ht PD signal. The reset of BCD counter is controlled by reset automatic block.[3]

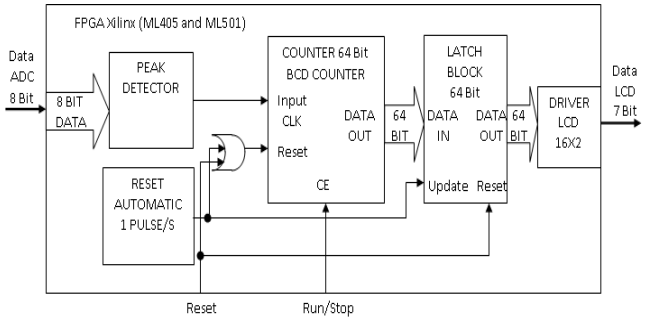

Figure 8 Block diagram of the connection of the FPGA to ADC and LCD of the complete pulse detection circuit system[2]

Figure 8 shows the block diagram of the connection for the FPGA to ADC and LCD of the complete pulse detection circuit system.[2]

3. The latch block in the hardware implementation of FPGA board:

The function of the latch block programming in this detection circuit system is for holding data from the output counter and reset block to display when the counter block is running. This will ensure that the display will keep the data to constant when the counter block is reset and return to zero again and counting again to update new data.[3]

After finishing the process of the latch block, the output data in this block will be sent to the driver of the LCD 16x2 character module.

4. The reset automatic block in hardware implementation of the FPGA Board:

The function of the reset automatic block is to generate impulse reset each of 1.0 sec that will be supplied to the counter block and latch block. It is very important because the data output from the latch block cannot be updated without this signal and also the data output from the BCD counter block cannot be reset without this signal. The timing of impulse reset signal can be changed using FPGA programming. In the real system the timing of impulse reset signal is set to 1.0 sec.[3]

5. The driver LCD Block in the hardware implementation of FPGA Board:

The function of the LCD block in the system is to display the text and counts into LCD display 16x2 character module. With this module, it is easy to read the amount of the pulses directly and this can give the indication whether the rate, amplitude or duration of the pulse is high.[3] There are 4 displays in the system:[4]

a. Display amount of PD signal in 1 second
b. Display signal input from ADC board without latch
c. Display real time data when counting using the peak detector.
d. Display signal input from ADC board with latch of 1.0 sec.

After finishing the process by the driver LCD block, the output data in this block will be sent to the LCD.[5]

The Impulse Generator

Figure 9 shows the impulse generator to simulate the PD signal when doing test PD detection circuit system in Lab simulation.[6] The Impulse generator can generate pulse of PD signal in Pico second until 100 ns and the amplitude of pulse from 4.5 mV to 50000 mV (50 Volt maximum) with repetition frequency from 10 KHz to 100 KHz.[3]

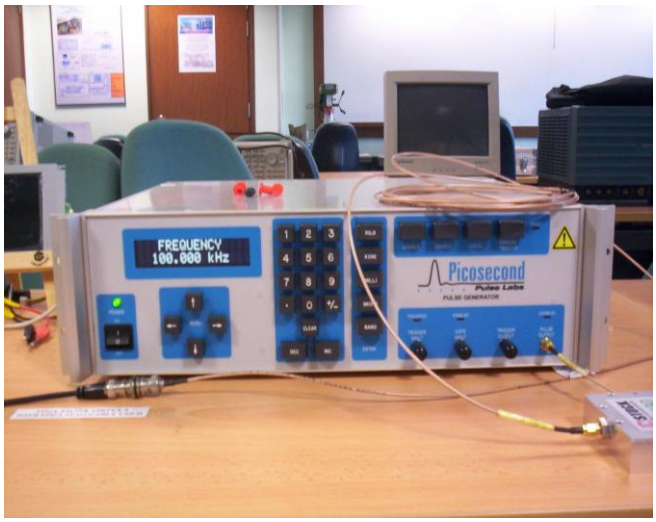

Figure 9 Impulse Generator of PD Detection System

The PD detection circuit was successfully tested in the laboratory using the impulse generator to simulate the PD signal.[7] The counts in the detection system are a function of the pulse amplitude, repetition frequency and pulse duration.[8] It has been shown that the counting system is also subjected to dead time effects.[9] This is a correction that will be incorporated in the future system. The PD detection circuit was successfully tested in the field to count real PD events. The tests were carried out in two companies. The system successfully detected PD signals. The counts were averaged at 6-7. From lab simulation, it can be inferred that the PD events in these installations are mild.[10]

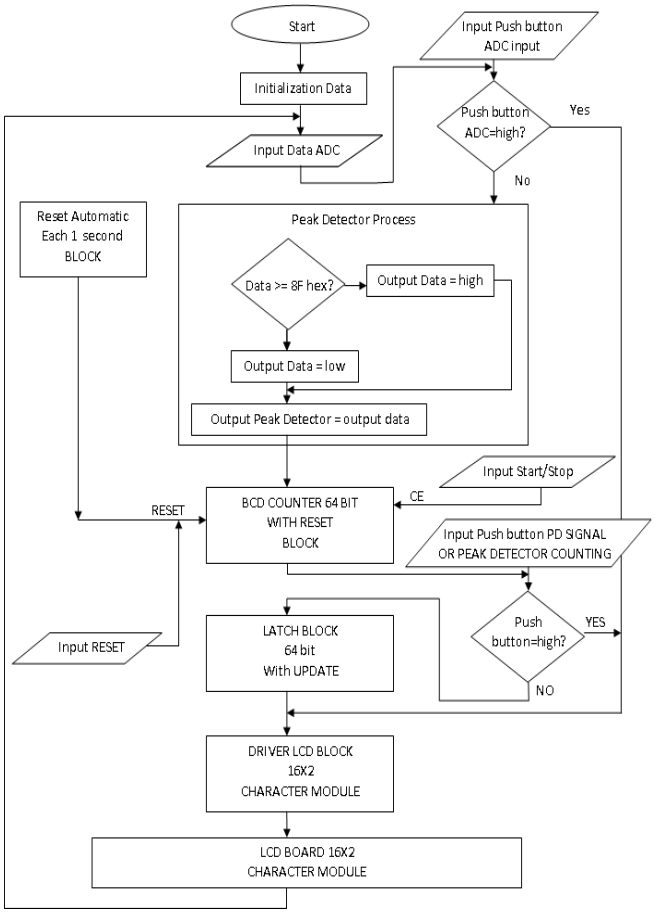

Figure 10 Flow chart of the complete pulse detection circuit system

Figure 10 shows the flow chart of the complete PD detection circuit system in FPGA board using VHDL programming.

4. THE SIMULATION RESULT

Simulation result for ADC with Peak Detector Block, BCD Counter and Reset Block, Reset Automatic Block and Latch Block Programming:

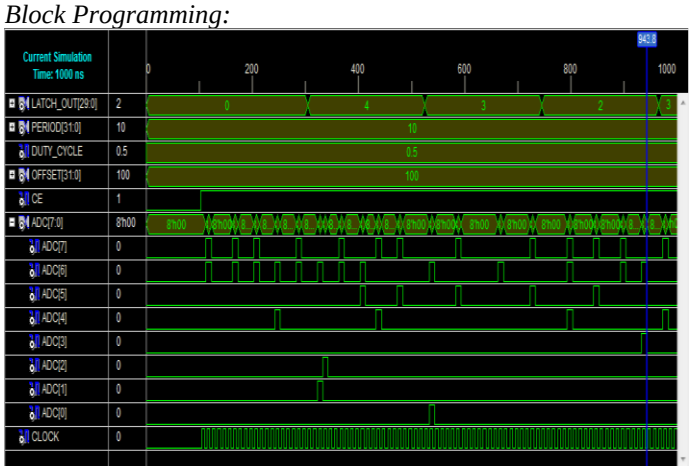

Figure 11 Simulation Results of Peak Detector Block, Counter Block, Reset Automatic Block and Latch Block.

Figure 11 shows the result of the simulation of PD detection circuit system consisting of combination ADC with Peak Detector Block, Counter with Reset Block, Reset Automatic Block and Latch block in FPGA programming using Xilinx ISE simulator 10.1. Figure 12 shows the graphic analysis of PD detection circuit system.

Graphic analysis of ADC with Peak Detector Block, Counter and Reset Block and Reset Automatic Block Programming:

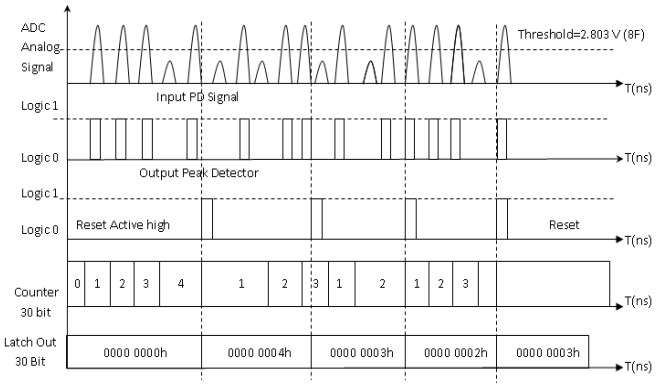

Figure 12 Analysis Simulation Results of Peak Detector Block, Counter Block, Reset Automatic Block and Latch Block.

Counter start to count PD Signal when the CE (Chip Enable) is high or Active. If the data of ADC signal is more than 2.8 mV or 11000100 bin then the counter will detect data and increase counting, but if the data of ADC signal is less than 2.8 mV or 11000100 bin then the counter will not detect data and data is not updated. Reset Automatic will reset to 220 ns, it is dependent on the timing set of reset automatic. Data output counter is held by latch block when the up counter is reset and counting again. The timing of timer automatic block can run constantly in latch block successfully and the up counter block can reset successfully**.** So the output of latch block can update the data constantly. The reset automatic is changed to 1 second in VHDL programming when implemented in the PD detection circuit system.

5. THE IMPLEMENTATION RESULT

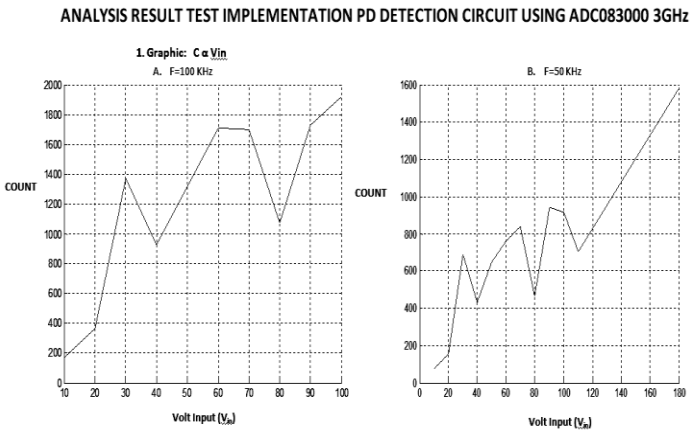

Figure 13 Results of Counting versus input pulse voltage at repetition frequency 100 KHz and 50 KHz

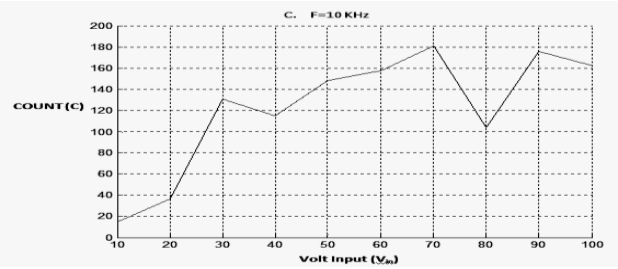

Figure 14 Results of Counting versus pulse input voltage at repetition frequency 10 KHz

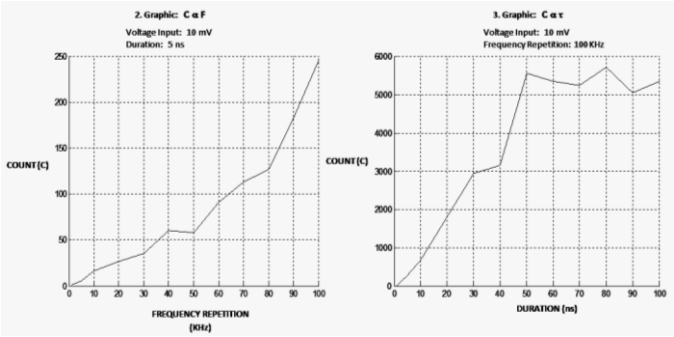

Figure 15 Results of Counting versus repetition frequency and Counting versus Duration

Graphic analysis for Implementation of PD Detection Circuit System Using Giga Hertz ADC.

a. Computation to find a constant value in *k*:
As the combination of the three variations has an empirical factor *k* that can be determine as follows,

$$C \alpha V_{in} \quad C = k.V_{in}.\tau.f$$
$$C \alpha \tau \quad C = 200$$
$$C \alpha f$$

$$V_{in} = 21\,mV \;;\quad f = 93KHz \;;\quad \tau = 2ns$$
$$k = \frac{C}{(V_{in}.\tau.f)} = \frac{200}{(0.021 * 93000 * 2 * 10^{-9})}$$
$$= 51203277 \ldots\ldots\ldots\ldots\ldots (1)$$

b. Hence the equation of relationship between Count signal and Actual signal:

$$C = k.V_{in}.\tau.f$$
$$C = 51203277 * 0.021 * 2.10^{-9}.f$$
$$C = 0.002151\,.f \quad \ldots\ldots\ldots\ldots\ldots (2)$$

$$if \quad V_{in} = 21\,mV \;;\; \tau = 2ns$$
$$C = Count\ signal \;;\; f = Actual\ signal$$

Figure 16 The Output of LCD in FPGA

Figure 13 and figure14 shows the graph of counts versus voltage input. Figure 15 shows the graph of counts versus repetition frequency and counts versus duration. Figure 16 show the output LCD of the implementation for the PD detection circuit in FPGA board. Equation (1) shows the computation to find the empirical factor *k* from the graphs. Equation 2 shows the relationship between the Count signal and the actual signal. This relationship is now able to just indicate the actual count irrespective of the any of the three variables.

6. CONCLUSION

The Combination of ADC and Peak Detector Block, Counter and Reset Block, Reset Automatic and Latch Block has been successful in the synthesis, compilation, simulation and implementation in FPGA. The combination block programming of the PD detection circuit system works successfully in FPGA compiler. A relationship has been deduce that has taken into account all the possible variables which directly influence the count.

7. REFERENCE

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